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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,750	03/04/2004	Kenji Takase	0951-0133P	5270
2292	7590	06/15/2006	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			HO, TU TU V	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/791,750

Applicant(s)

TAKASE, KENJI

Examiner

Tu-Tu Ho

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 13-15 and 21-23 is/are pending in the application.
- 4a) Of the above claim(s) 8-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 21-23 is/are rejected.
- 7) ☒ Claim(s) 5-7 and 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/ Restriction

1. Applicant's election with traverse of Species I, claims 1-7, 13-15, and 21-23, in the reply filed on 05/25/2006 is acknowledged. The traversal is on the ground(s):

(i) It cannot be determined from the Office Action whether the examiner is requiring restriction between two independent and distinct inventions or is making an election of species requirement;

(ii) "Claims are never species" as quoted by Applicant from MPEP 806.04(e);

(iii) The record in no manner shows or suggests that different species are disclosed;

(iv) Explain which drawing figures show the first species and which drawing figures show the second species so that Applicant can better understand this requirement; and

(v) It has not been shown that maintaining all claims in this application would constitute a serious burden on the examiner.

This is not found persuasive because:

(i) The requirement is mainly about species. Nevertheless, MPEP 806.04(b) [R-3] also provides:

"Where inventions as disclosed and claimed are both (A) species under a claimed genus and (B) related, then the question of restriction must be determined by both the practice applicable to election of species and the practice applicable to other types of restrictions"

And as such, the practice of “intermediate and final product” is practiced in the paragraph bridging pages 2 and 3 of the office action mailed 04/27/2006;

(ii) Although MPEP 806.04(e) states: “Claims are never species”, MPEP does not state that patently distinct species are not identifiable by claims. Specifically, the whole section is as follows:

“

806.04(e) [R-3] Claims *>Limited< to Species

Claims are definitions of inventions. Claims are never species. *>The scope of a claim< may be *>limited< to a single disclosed embodiment (i.e., a single species, and thus be designated a specific species claim), or a claim may include two or more of the disclosed embodiments within the breadth and scope of *>the claim< (and thus be designated a generic or genus claim).

Species are always the specifically different embodiments.

Species **>may be either< independent >or related< as disclosed (see MPEP § 806.04 and § 806.04(b)) **.

“

(iii) As noted above in (ii), patently distinct species are identifiable by claims, thus the record has showed or suggested that different species are disclosed;

(iv) As noted above in (ii), although MPEP 806.04(e) states “Claims are never species”, MPEP does not state that patently distinct species are not identifiable by claims; therefore, patently distinct species are identifiable by claims. However, for the sake of being responsive to

the argument, Fig. 1 and 2, for example, show the first species, and Figs. 5 and 6, for example, show the second species; and

(v) Maintaining all claims in this application would constitute a serious burden on the examiner, because a reference anticipates species I, for example, would not necessarily anticipate species II, forcing the examiner to spend more time for searching.

The requirement is still deemed proper and is therefore made FINAL.

2. **Claims 8-10** are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 05/25/2006, as noted above.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “circuit board” of **claim 22** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. **Claim 5** (misabeled as second claim 4) is objected to because of the following informalities: claim 5 is mislabeled as claim 4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 1 and 21-23** are rejected under 35 U.S.C. 102(e) as being anticipated by Horio et al. U.S. Patent 6,590,152 (the '152 reference, cited in a previous office action).

The '152 reference discloses in the figures, particularly Fig. 3, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device in which one semiconductor chip (2C, Fig. 4, col. 5, lines 1+) has been mounted onto a front surface of one substrate (10) having a front face, a rear face and one or more side faces connecting said front

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face and rear face, said substrate incorporating patterned wiring (generally indicated at 12a) and the entirety of the one semiconductor chip has been sealed with one resin (11) - meeting the claimed limitation one or more semiconductor chips have been mounted onto front faces of one or more substrates having front faces, rear faces and one or more side faces connecting said front faces and rear faces, said substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins - wherein:

one or more electrically conductive patterns (3, “shield cap”, col. 6, lines 29-40; because shield cap 3 may be formed by a thin metal plate, which plate is a pattern, and which metal is electrically conductive as is known, col. 6, lines 29-40, metal shield cap 3 is fairly termed an electrically conductive pattern) for shielding (“shield cap”) is or are formed at said one or more side faces of said one substrate – meeting the claimed limitation at least one of the substrate or substrates.

Referring to **claim 21** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device comprising:

a substrate incorporating patterned wiring and having a first surface, a second surface generally parallel to said first surface, and at least one peripheral edge surface connecting said first surface and said second surface;

one or more semiconductor chips mounted on said first surface and sealed with one or more resins; and

an electrically conductive shielding pattern at at least a portion of said at least one peripheral edge surface.

Referring to **claim 22**, the reference further discloses that said at least one peripheral edge comprises a first peripheral edge (generally defined at 12c, best seen in Figs. 5 and 2) having terminals (12c) for connecting said semiconductor device to a circuit board (not shown, col. 5, lines 23-35) and a second edge (generally defined at 30, fig. 5) spaced from said first edge, wherein said electrically conductive shielding pattern (3) covers said second edge (best seen in Fig. 6).

Referring to **claim 23**, the reference further discloses that said at least one peripheral edge comprises a first edge, a second edge parallel to said first edge and third and fourth edges connecting said first and second edges, wherein said electrically conductive shielding pattern is formed on one of said first, second, third and fourth edges (best seen in Fig. 5).

6. Claims 1 and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Egawa U.S. Patent 5,668,406 (the '406 reference).

The '406 reference discloses in Fig. 2A and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device in which one semiconductor chip (12, Fig. 2A, col. 2, lines 36+) has been mounted onto a front surface of one substrate (100) having a front face (generally defined by a face on which the IC chip 12 is mounted and which face is opposite to a rear face that is generally indicated by ground pattern 18), a rear face and one or more side faces connecting said front face and rear face, said substrate

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incorporating patterned wiring (generally indicated at 9) and the entirety of the one semiconductor chip has been sealed with one resin (13) - meeting the claimed limitation one or more semiconductor chips have been mounted onto front faces of one or more substrates having front faces, rear faces and one or more side faces connecting said front faces and rear faces, said substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins - wherein:

one or more electrically conductive patterns (generally indicated at ground electrode pattern 17, 17A & 18, col. 3, lines 22+) for shielding is or are formed at said one or more side faces of said one substrate – meeting the claimed limitation at least one of the substrate or substrates.

Referring to **claim 21** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device comprising:

a substrate incorporating patterned wiring and having a first surface, a second surface generally parallel to said first surface, and at least one peripheral edge surface connecting said first surface and said second surface;

one or more semiconductor chips mounted on said first surface and sealed with one or more resins; and

an electrically conductive shielding pattern at at least a portion of said at least one peripheral edge surface.

Referring to **claim 22**, the reference further discloses that said at least one peripheral edge comprises a first peripheral edge (generally defined at an edge covered by 17 or 17A)

having terminals (17 or 17A) for connecting said semiconductor device to a circuit board (for the device to function) and a second edge (generally defined at an edge covered by 17A or 17) spaced from said first edge, wherein said electrically conductive shielding pattern (17 or 17A) covers said second edge.

Referring to **claim 23**, the reference further discloses that said at least one peripheral edge comprises a first edge, a second edge parallel to said first edge and third and fourth edges connecting said first and second edges, wherein said electrically conductive shielding pattern is formed on one of said first, second, third and fourth edges.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. **Claim 2** is rejected under 35 U.S.C. §103(a) as being unpatentable over Egawa U.S. Patent 5,668,406 (the '406 reference), as evident by Terui U.S. Patent 6,060,774.

Referring to **claim 2**, the '406 reference discloses a semiconductor device substantially as claimed and as detailed above for claim 1 including the electrically conductive pattern (17,17A, 18) but does not teach that the electrically conductive pattern is a copper foil pattern as claimed.

However, copper foil, being an electrically conductive material, is a known and available material for forming an electrically conductive pattern for semiconductor devices, as is evident in the Terui reference (col. 1, lines 10-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that its electrically conductive pattern is

a copper foil pattern. One would have been motivated to utilize such a known and available material for forming an electrically conductive pattern for semiconductor devices, as is evident in the Terui reference.

8. **Claims 3-4** are rejected under 35 U.S.C. §103(a) as being unpatentable over Egawa U.S. Patent 5,668,406 (the '406 reference) as applied to claim 2 above, and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492 (cited in a previous office action).

The '406 reference discloses a semiconductor device substantially as claimed and as detailed above including the known-and-available copper foil or the least one of the known-and-available copper foil pattern or patterns, but does not teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the '327 reference such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the copper foil.

Allowable Subject Matter

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9. **Claims 5-7 and 13-15**, insofar as in compliance with the claim objections noted above, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device having all exclusive limitations as recited in claims 5, 7, 13, and 14.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 7:30 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tu-Tu Ho
June 08, 2006